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EXAMINER	
HUA, LY	

ART UNIT	PAPER NUMBER
2135	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,304	OISHI ET AL.	
	Examiner	Art Unit	
	Ly V. Hua	2135	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/25/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings Objection

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following element(s) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. The Figures of the Drawings do not show:
   a. the "lower-layer device" recited in claims 7 and 11.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> . The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-5 and 6-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. With regard to claims 2-5:
   a. The word "An" at the beginning of each of these claims is being misused and therefor is not idiomatic. Notice that each of these claims refers to the authentication communicating semiconductor device in its respective parent claim. The applicant is to replace each of the instance of the word "An" with –the—.

6. With regard to claim 6:
   a. The phrase "said each interface section" lacks antecedent basis.

7. With regard to claim 7:
   a. The word of article "an" for "an RAM" and for "an ROM" is not idiomatic. The word "an" in each of those instances should be changed to – a -- .
   b. In the clause "said lower-layer interface unit comprises at least one lower-layer communication path for communicating encrypted statement data with a lower-layer device controlling a communication signal outside said semiconductor chip" is confusing and cannot be understood. The following problems are listed to define why the clause is confusing:
      i The subject that uses the at least one lower-layer communication path for communicating encrypted statement data with a lower-layer device is not clear.
      ii It appears that certain text(s) is/are missing between the words "signal" and "outside".
      iii It is not clear whether the modifier "controlling a communication signal" is used to modify the lower-lay device or to modify the lower-lay interface unit.
      iv The "lower-layer device" cannot be found in the drawing to determine what it is.
      v It is not clear whether the phrase "outside said semiconductor chip" is used to modify the lower-layer device or the controlling or the communication signal.

8. With regard to claim 8-11, and 12:
   a. These claims depend on claim 7 and thus inherit the problem of indefiniteness therefrom.

9. With regard to claims 8-11:
   a. The word "An" at the beginning of each of these claims is being misused and therefor is not idiomatic. Notice that each of these claims refers to the authentication communicating semiconductor device in its respective parent claim. The applicant is to replace each of the instances of the word "An" with –the—.

10. With regard to claim 8:
    a. The usage of prepositional words "between" and "to" in the phrase "a second ... path between said lower-layer interface unit to said upper-layer interface unit" is not idiomatic. The applicant is either to use –between— and –and-- , or to use – from – and – to -.

11. With regard to claim 10:
    a. This claim depends on claim 8 and thus inherits the problem of indefiniteness therefrom.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
.(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-7, 9, 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Figure 13, 14 and the description thereof in applicant's specification) in view of Miyazaki et al (6,466,668 hereinafter Miyazaki) .

14. Claim 1 claims an authentication communicating semiconductor device,
    a. comprising:
        i a semiconductor chip;
        ii a main processing unit
            (1) formed on said semiconductor chip
            (2) for generating
                (a) a key code
                (b) according to a predetermined algorithms
            (3) for determining approval/non-approval
                (a) of communication of data with an external device, and
            (4) for controlling the communication;
        iii an encryption unit
            (1) formed on said semiconductor chip
            (2) for encrypting and decoding
                (a) communication data
                (b) using the key code generated by said main processing unit;
        iv a first interface unit
            (1) formed on said semiconductor chip
            (2) for conducting communication
                (a) with an upper layer
                (b) according to a predetermined protocol; and
        v a second interface unit
            (1) formed on said semiconductor chip
            (2) for conducting communication
                (a) with a lower layer
                (b) according to a predetermined protocol.

15. Claim 13 claims an authentication communicating semiconductor device,
    a. comprising:
        i a semiconductor chip;
        ii a main processing unit
            (1) formed on said semiconductor chip
            (2) for generating
                (a) a key code
                (b) according to a predetermined algorithm,
            (3) for determining approval/non-approval
                (a) of communication of data with an external device, and
            (4) for controlling the communication;
        iii an encryption unit
            (1) formed on said semiconductor chip
            (2) for encrypting and decoding
                (a) communication data
                (b) using the key code generated by said main processing unit; and
        iv an interface unit
            (1) formed on said semiconductor chip
            (2) for conducting communication
                (a) with an upper-layer or a lower-layer
                (b) according to a predetermined protocol.

16. As to claims 1, and 13:
    a. Applicant's admitted prior art teaches an authentication communicating semiconductor device [Fig. 13], comprising:
        i a semiconductor chip [72];
        ii a main processing unit [500]
            ~~(1) formed on said semiconductor chip~~
            (2) for generating
                (a) a key code
                (b) according to a predetermined algorithms
            (3) for determining approval/non-approval
                (a) of communication of data with an externa device, and
            (4) for controlling the communication;
        iii an encryption unit [300]
            (1) formed on said semiconductor chip
            (2) for encrypting and decoding
                (a) communication data
                (b) using the key code generated by said main processing unit;
        iv a first interface unit [200]
            (1) formed on said semiconductor chip
            (2) for conducting communication
                (a) with an upper layer
                (b) according to a predetermined protocol; an
        v a second interface unit [300]
            (1) formed on said semiconductor chip
            (2) for conducting communication
                (a) with a lower layer
                (b) according to a predetermined protocol.
    b. However, Applicant's admitted prior art does not show t the main processing unit [500] is formed on the semiconductor chip [72]. This is because Applicant's admitted prior art formed the main processing unit [500 on another semiconductor chip [71].
    c. Miyazaki et al (6,466,668 hereinafter Miyazaki) teaches:
        i forming a processing unit [101] on a semiconductor chip [101] that has encryption unit [107], and interface units [105] and does encryption.
    d. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:
        i form the main processing unit of Applicant's admit prior art in the semiconductor chip [72].
    e. The skilled person would have been motivated to do suc formation because:
        i Applicant's admitted prior art teaches that the main processing unit [500] can be formed on a semiconductor chip [71]; and
        ii Miyazaki teaches that processing unit can be forme on a semiconductor chip that includes:
            (1) encryption unit, and
            (2) input/output interface units;
        iii merging the components from a plurality of chips in a single chip would have been obvious to a person having the ordinary skill in the art since the advancement in the semiconductor art has enable a plurality of semiconductor chip elements to be implemented on a single chip; and
        iv the skilled person in the art would have realized tha in the device 800 of applicant's admitted prior art, combination of the bus in element 71, bus 41 and th bus in element 72 is a single bus node.

17. Claim 2 claims:
    a. 2. An authentication communicating semiconductor device according to claim 1, wherein

        i said main processing unit comprises:

            (1) a nonvolatile memory
                (a) having stored therein
                    (i) a program implementing a key generation algorithm and
                    (ii) an authentication algorithm to authenticate an external device requesting data communication;

            (2) program-execution-type control means
                (a) for generating a key code and
                (b) for determining approval/non-approval of communication of data with an external device according to the program; and

            (3) a volatile memory
                (a) for providing
                    (i) a work area
                    (ii) for
                        1) said control means,
                        2) said nonvolatile memory,
                        3) said control means,
                        4) said volatile memory,
                        5) said encryption unit, and

        ii said first and second interface units being connected to each other via an internal bus.

18. As to claim 2:
    a. Applicant's admitted prior art teach that in the authentication communicating semiconductor device [Figure 13],

        i said main processing unit [500] comprises:

            (1) a nonvolatile memory [501]
                (a) having stored therein
                    (i) a program implementing a key generation algorithm and
                    (ii) an authentication algorithm to authenticate an external device requesting data communication;

            (2) program-execution-type control means [which is inherent in element 500 since element 500 is to generate a key code and to determine whether to approve or to deny a communication of data – (Specification, the paragraph bridging pages 4 and 5)]
                (a) for generating a key code and
                (b) for determining approval/non-approval of communication of data with an external device according to the program; and

            (3) a volatile memory [502]
                (a) for providing
                    (i) a work area
                    (ii) for
                        1) said control means,
                        2) said nonvolatile memory,
                        3) said control means,
                        4) said volatile memory,
                        5) said encryption unit, and

        ii said first and second interface units [100, 200] being connected to each other via an internal bus [i.e., the bus connecting elements 100 and 200 of the applicant's admitted prior art].

19. Claim 3 claims:

    a. 3. An authentication communicating semiconductor device according to claim 2 wherein:

        i said encryption unit includes

            (1) a register
                (a) to which the key code generated by said main processing unit
                    (i) is set; and

        ii said encryption unit encrypts and decodes
            (1) communication data
            (2) according to the key code
                (a) set
                    (i) via said internal bus
                    (ii) to said register.

20. As to claim 3:

    a. Applicant's admitted prior art teaches that in the authentication communicating semiconductor device [Figure 13],

        i said encryption unit [300] includes
            (1) a register [34]
                (a) to which the key code generated by said main processing unit
                    (i) is set [by element 50 via element 41] ; and

        ii said encryption unit [300] encrypts and decodes
            (1) communication data
            (2) according to the key code
                (a) set
                    (i) via said internal bus [connecting elements 100, 200, 300 in element 72 to element 41 and to element 50]
                    (ii) to said register [34].

21. Claim 4 claims:
    a. 4. An authentication communicating semiconductor device according to claim 3, wherein:

        i each of said first and second interface units
            (1) includes a register to which a communication code is set; and

        ii each interface unit conducts communication
            (1) according to
                (a) a communication control code
                    (i) set
                        1) by said main processing unit
                        2) via said internal bus
                        3) to said register.

22. As to claim4:
    a. Applicant's admitted prior art teaches that in the authentication communicating semiconductor device [Figure 13],

        i each of said first and second interface units [100, 200]
            (1) includes a register [14, 24] to which a communication code is set; and

        ii each interface unit conducts communication
            (1) according to
                (a) a communication control code
                    (i) set
                        1) by said main processing unit [500]
                        2) via said internal bus [connecting elements 100, 200, 300 in element 72 to element 41 and to element 50]
                        3) to said register [14, 24].

23. Claim 5 claims:
    a. 5. An authentication communicating semiconductor device according to claim 4 further comprising

        i an external terminal

            (1) coupled with said internal bus.

24. As to claim 5:
    a. Applicant's admitted prior art teaches that the authentication communicating semiconductor device [Figure 13] further comprising:

        i an external terminal [i.e., the segment for which elements 740 and 750 can be connected to the single chip formed by obviously combining element 71 and 72 as reasoned above in the rationale for rejecting claim 1 above]

            (1) coupled with said internal bus [connecting elements 100, 200, 300 in element 72 to element 41 and to element 50].

25. Claim 6 claims:
    a. 6. An electronic device,

        i comprising:

            (1) an authentication communicating semiconductor device according to claim 5; and

            (2) an external memory
                (a) connected
                    (i) to said external terminal connect to said internal bus;

        ii wherein:

            (1) a communication control program
                (a) includes setting of a communication path
                (b) is stored in said external memory; and

            (2) said main processing unit
                (a) sets
                    (i) according to a communication code
                    (ii) said communication control program
                    (iii) to said register
                        1) of said each interface section
                            a) to conduct communication with an external device.

26. As to claim 6:
    a. Applicant's admitted prior art teaches [Figure 13] an electron device 800,

        i comprising:

            (1) an authentication communicating semiconductor device according to claim 5 [i.e., the combination of element 71 and 72 into a single chip maintaining the function of element 71 and the function of element 72, which combination has been addressed above in the rejection of claim 1 with reference to Applicant's admitted prior art and Miyazaki et al (6,466,668)]; and

            (2) an external memory [740]
                (a) connected
                    (i) to said external terminal [which has been pointed out in the rejection of claim 5 above] connect to said internal bus;

        ii wherein:

            (1) a communication control program
                (a) includes setting of a communication path
                (b) is stored in said external memory [740] ; and

            (2) said main processing unit [500]
                (a) sets
                    (i) according to a communication code
                    (ii) said communication control program
                    (iii) to said register [14, 24]
                        1) of said each interface section [100, 200]
                            a) to conduct communication with an external device.

27. Claim 7 claims an authentication communicating semiconductor device,
    a. comprising:

        i a single semiconductor chip;

        ii an encryption unit
            (1) formed on said single semiconductor chip
            (2) for encrypting,
                (a) in an encrypting mode,
                (b) ordinary or non-encrypted statement data
                (c) into encrypted statement data;
            (3) for decoding,
                (a) in a decoding mode,
                (b) the encrypted statement data
                (c) into ordinary statement data; and
            (4) for directly passing
                (a) data
                (b) there through
                (c) when nether encryption nor decoding is required;
        iii a lower-layer interface unit
            (1) formed on said single semiconductor chip
            (2) for the encrypted statement data of said encryption unit for controlling a protocol of communication with a lower layer;
        iv an upper-layer interface unit
            (1) formed on said single semiconductor chip
            (2) for the ordinary statement data of said encryption unit for controlling a protocol of communication with an upper layer; and
        v a key generation unit
            (1) formed on said single semiconductor chip
            (2) for executing authentication processing of communication passing through the lower layer and
            (3) for executing key generation processing for said encryption unit,

        vi wherein:

            (1) said lower-layer interface unit comprises
                (a) at least one lower-layer communication path
                    (i) for communicating
                        1) encrypted statement data
                        2) with a lower-layer device
                            a) controlling a communication signal
                        3) outside said semiconductor chip;

            (2) said upper-layer interface unit comprises
                (a) at least one upper-layer communication path
                    (i) for communicating
                        1) ordinary statement data
                        2) with an upper-layer device
                            a) outside said semiconductor chip;
            (3) said key generation unit comprises
                (a) a CPU,
                (b) an ROM, and

28. As to claim 7, Applicant's admitted prior art teaches an authentication communicating semiconductor device,
    a. comprising:
        i a single semiconductor chip [i.e., a combination of elements 71 and 72 in a single chip, the forming of which single chip is obvious as addressed above in the rejection of claim 1 with reference to Applicant's admitted prior art in view of Miyazaki];
        ii an encryption unit [300]
            (1) formed on said single semiconductor chip
            (2) for encrypting,
                (a) in an encrypting mode,
                (b) ordinary or non-encrypted statement data
                (c) into encrypted statement data;
            (3) for decoding,
                (a) in a decoding mode,
                (b) the encrypted statement data
                (c) into ordinary statement data; and
            (4) for directly passing
                (a) data
                (b) there through
                (c) when nether encryption nor decoding is required;
        iii a lower-layer interface unit [100]
            (1) formed on said single semiconductor chip
            (2) for the encrypted statement data of said encryption unit for controlling a protocol of communication with a lower layer;
        iv an upper-layer interface unit [200]
            (1) formed on said single semiconductor chip
            (2) for the ordinary statement data of said encryption unit for controlling a protocol of communication with an upper layer; and
        v a key generation unit [element 50 from element 71 which is moved and merged into element 72, which moving and merging is obvious over Applicant's admitted prior in view of Miyazaki as has been presented above]
            (1) formed on said single semiconductor chip [after the obvious moving and merging have been obviously made]
            (2) for executing authentication processing of communication passing through the lower layer and
            (3) for executing key generation processing for said encryption unit,
        vi wherein:
            (1) said lower-layer interface unit[100] comprises
                (a) at least one lower-layer communication path [11]
                    (i) for communicating
                        1) encrypted statement data [from element 300]
                        2) with a lower-layer device [i.e., a combination of elements 12, 700 and 720,]
                            a) [which combination of elements 12, 700 and 720 are for] controlling a communication signal [to or from the] outside [of] said semiconductor chip;
            (2) said upper-layer interface unit [200] comprises
                (a) at least one upper-layer communication path [22]
                    (i) for communicating
                        1) ordinary statement data
                        2) with an upper-layer device [90]
                            a) outside said semiconductor chip;
            (3) said key generation unit comprises
                (a) an ROM [501], and
                (b) an RAM [502] ; and

(c) an RAM; and (4) said CPU (a) sets (i) a key register for said encryption unit to hold an encryption key, (ii) a control register of said lower-layer interface unit, and (iii) a control register of said upper-layer interface unit (iv) via a bus connecting 1) said CPU, 2) said encryption unit, 3) said lower-layer interface unit, and 4) said upper-layer interface unit 5) to each other.	(c) a CPU [500], (4) said CPU [500] (a) sets (i) a key register [34] for said encryption unit [300] to hold an encryption key, (ii) a control register [14] of said lower-layer interface unit [100], and (iii) a control register [24] of said upper-layer interface unit [200] (iv) via a bus [i.e., the bus originally connecting elements 100, 200 and 300 and additionally connecting elements 50 to those elements 100, 200 and 300 after the obvious moving and merging have been made {notice the even before the moving and merging have been made element 50 and elements 100, 200 and 300 share the same nodes (which same node being the combination of connected bus 41, internal bus of element 71 and internal bus of element 72)}] connecting 1) said CPU [500], 2) said encryption unit [300], 3) said lower-layer interface unit [100], and 4) said upper-layer interface unit [200] 5) to each other.

29. Claim 11 claims an authentication communicating semiconductor device according to claim 7, wherein a. said lower-layer device is formed on said semiconductor chip, b. said authentication communicating semiconductor device further comprising i at least one communication path (1) for communicating signals with said lower-layer device.	30. As to Claim 11, applicant's admitted prior art teaches an authentication communicating semiconductor device according to claim 7, wherein a. said lower-layer device is formed on said semiconductor chip, b. said authentication communicating semiconductor device further comprising i at least one communication path [12] (1) for communicating signals with said lower-layer device.

31. Claim 9 claims an authentication communicating semiconductor device according to claim 7 wherein:

    a. said encryption unit comprises
        i a first encryption circuit and
        ii a second encryption circuit; and

    b. said upper-layer interface unit includes
        i a first upper-layer interface unit and
        ii a second upper-layer interface unit,

    c. said communication path
        i of the ordinary statement data
            (1) of said first encryption circuit
        ii being connected to said first upper-layer interface circuit,

    d. said communication path
        i of the ordinary statement data
            (1) of said second encryption circuit
        ii being connected to said second upper-layer interface circuit,

    e. said first upper-layer interface unit including
        i a first upper-layer communication path
            (1) for communicating
                (a) signals
                (b) with a first upper-layer device
                    (i) outside said semiconductor chip,

    f. said second upper-layer interface unit including
        i a second upper-layer communication path
            (1) for communicating
                (a) signals
                (b) with a second upper-layer device
                    (i) outside said semiconductor chip.

32. As to claim 9, applicant's admitted prior art [Figure 13] teaches an authentication communicating semiconductor device according to claim 7 wherein:

    a. said encryption unit [300] comprises
        i a first encryption circuit [34] and
        ii ~~a second encryption circuit~~; and

    b. said upper-layer interface unit includes
        i a first upper-layer interface unit and
        ii ~~a second upper-layer interface unit~~,

    c. said communication path
        i of the ordinary statement data
        ii of said first encryption circuit
        iii being connected to said first upper-layer interface circuit,

    ~~d. said communication path~~
        ~~i of the ordinary statement data~~
        ~~ii of said second encryption circuit~~
        iii ~~being connected to said second upper-layer interface circuit,~~

    e. said first upper-layer interface unit including
        i a first upper-layer communication path
            (1) for communicating
                (a) signals
                (b) with a first upper-layer device
                    (i) outside said semiconductor chip,

    ~~f. said second upper-layer interface unit including~~
        ~~i a second upper-layer communication path~~
            ~~(1) for communicating~~
                ~~(a) signals~~
                ~~(b) with a second upper-layer device~~
                    (i) ~~outside said semiconductor chip~~.

33. However, Applicant's admitted prior art does not show:
    a. the second encryption circuit;
    b. the second upper-layer interface unit;
    c. that the communication path of the ordinary statement data of the second encryption circuit being connected to the second upper-layer interface circuit; and
    d. the second upper-layer interface unit including a second upper-layer communication path for communicating signals with a second upper-layer device outside said semiconductor chip.

34. Viewing the structure of claim 9, it is seen that the structure is a modification of Prior Art Figure 13. The modification being that some of the elements (particularly the elements listed above as not being shown by Applicant's admitted prior art) in the chip 72 of the Prior Art are provided redundantly and connected in parallel to yield a parallel effect.

35. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide and connect the same combination of certain elements in parallel to provide the same parallel effect for purposes of duplications and/or reliability.

36. The skilled person would have been motivated to do such provision and connection because such technique for parallel/redundant effect for purpose of duplications/reliability is commonly used in the art.

Ojbections

37. Claims 8 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. Claims 8 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

39. The following is a statement of reasons for the indication of allowable subject matter:

40. Claim 8 claims an authentication communicating semiconductor device according to claim 7, further comprising:

a. a first upper-layer-lower-layer communication path and

b. a second upper-layer-lower-layer communication path
   i between
      (1) said lower-layer interface unit
      (2) to said upper-layer interface unit
   ii without passing said encryption unit,

c. said upper-layer interface unit comprising
   i a first upper-layer communication path and
   ii a second upper-layer communication path
      (1) for communicating
         (a) signals
         (b) with an upper-layer device
            (i) outside said semiconductor chip,

d. said first upper-layer communication path
   i being capable of selecting
      (1) data
         (a) from said encryption unit and
      (2) data
         (a) from said lower-layer interface unit said upper-layer interface unit
      (3) without passing through said encryption unit,

e. said second upper-layer communication path
   i being capable of selecting
      (1) data
         (a) from said first upper-layer-lower-layer communication path and
      (2) data
         (a) from said second upper-layer-lower-layer communication path.

f. Claim 10 claims an authentication communicating semiconductor device according to claim 8, further comprising an electrically rewritable nonvolatile memory formed on said semiconductor chip, said memory being connected to said internal bus.

41. As to claims 8 and 10, applicant's admitted prior art teaches an authentication communicating semiconductor device according to Applicant's Prior Art Figure 13, further comprising:

a. a first upper-layer-lower-layer communication path [i.e., the path including elements 11, 300 and 21] and

~~b. a second upper-layer-lower-layer communication path between~~
   ~~(1) said lower-layer interface unit [100]~~
   ~~(2) to said upper-layer interface unit [200]~~
   ii ~~without passing said encryption unit,~~

c. said upper-layer interface unit [200] comprising
   i a first upper-layer communication path [21] and
   ii a second upper-layer communication path [22]
      (1) for communicating
         (a) signals
         (b) with an upper-layer device [90]
            (i) outside said semiconductor chip,

~~d. said first upper-layer communication path [21]~~
   ~~i being capable of selecting~~
      ~~(1) data~~
         ~~(a) from said encryption unit and~~
      ~~(2) data~~
         ~~(a) from said lower-layer interface unit said upper-layer interface unit~~
      (3) ~~without passing through said encryption unit,~~

e. said second upper-layer communication path [22]
   i being capable of selecting
      (1) data [i.e., encrypted communication data]
         (a) from said first upper-layer-lower-layer communication path and
      (2) data [i.e., control data]
         (a) from said second upper-layer-lower-layer communication path [i.e., the chip's internal bus].

f. an electrically rewritable nonvolatile memory [RAM 502 which can be obvious be moved and implemented in the chip 72 of Applicant's Admitted Prior Art to form a single chip (as have been said above in the rejection of claim 1 to be obvious over Applicant's admitted prior art in view of Miyazaki)
   i formed on said semiconductor chip [after the moving and the implementation],
   ii said memory being connected to said internal bus.

42. However, Applicant's admitted prior art and Miyazaki doe not teach the limitations of b and d (which are shown crossed out above) in combination with the rest of the other limitations of claim 8.

43. The prior art of record also fail to teach or suggest such limitation.

44. Claims 8 and 10 are thus allowable over the prior art of record.

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly V. Hua whose telephone number is 571-272-3853. The examiner can normally be reached on Monday to Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Kim, can be reached on 571-272-3858. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

47. The applicant is hereby notified that:
a. The new phone number for TC 2100 receptionist is (571) 272-2100.

Ly V. Hua
Primary Examiner
Art Unit 2135

Lvh
December 8, 2004